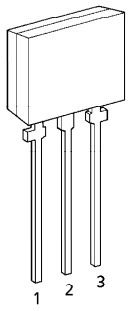
TOSHIBA INTELLIGENT POWER DEVICE SILICON MONOLITHIC POWER MOS INTEGRATED CIRCUIT

TPD1024AS

LOW-SIDE POWER SWITCH for MOTORS, SOLENOIDS, and LAMP DRIVERS

TPD1024AS is a monolithic power IC for low-side switches. The IC has a vertical MOS FET output which can be directly driven from a CMOS or TTL logic circuit (e.g, an MPU). The device offers intelligent self-protection function.



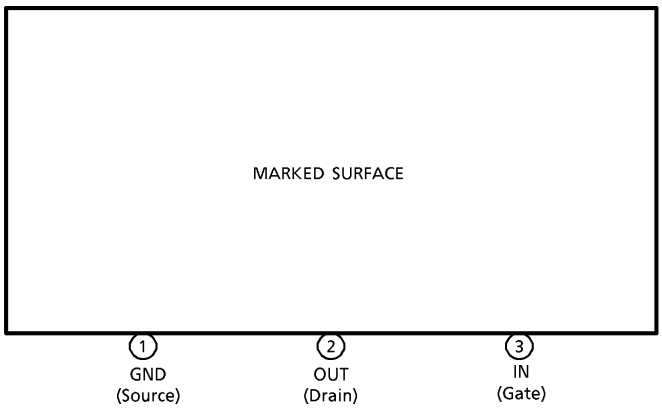
SIP3-P-2.50

Weight : 0.54 g (Typ.)

FEATURES

- A monolithic power IC with a new structure combining a control block and a vertical power MOS FET (π-MOS) on a single chip.
- Can directly drive a power load from a CMOS logic.
- Built-in protection against overvoltage, load short circuiting, and overheating.
- Low on resistance : $R_{DS\,(ON)}$ = 0.5 Ω (Max), @V_{IN} = 5 V, T_j = 25°C
- Package : TPS Can be packed in tape.

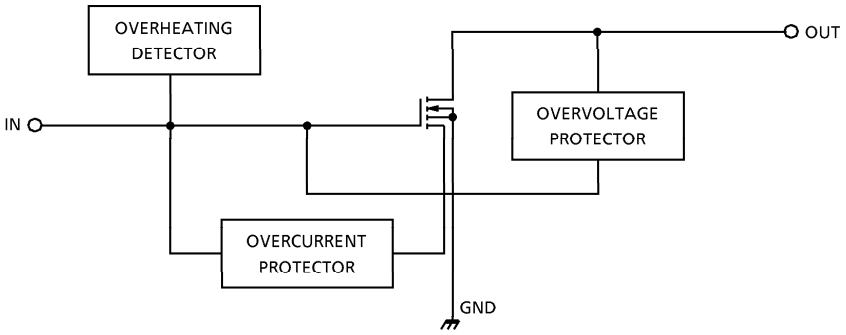
PIN ASSIGNMENT



(Note) : That because of its MOS structure, this product is sensitive to static electricity.

980910EBA1

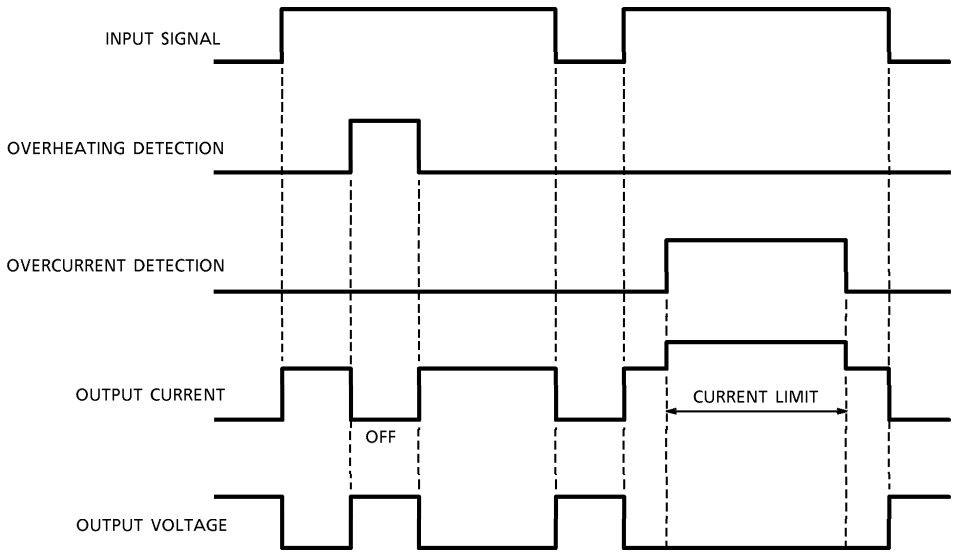
BLOCK DIAGRAM



PIN DESCRIPTION

PIN No.	SYMBOL	FUNCTION
1	GND	Ground pin.
2	OUT	Output pin. When current in excess of the typical current (3.5 A) flows to the output pin, the current limiter operates to protect the IC.
3	IN	Input pin. Input is CMOS-compatible, with pull-down resistor connected. Even if the input is open, output will not accidentally turn on.

TIMING CHART



MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Drain-source Voltage	$V_{DS\ (DC)}$	40	V
Output Current	I_D	1.5	A
Input Voltage	V_{GS}	−0.5~6	V
Power Dissipation	P_D	1.2	W
Operating Temperature	T_{opr}	−40~85	°C
Junction Temperature	T_j	150	°C
Storage Temperature	T_{stg}	−55~150	°C

RECOMMENDABLE CONDITION

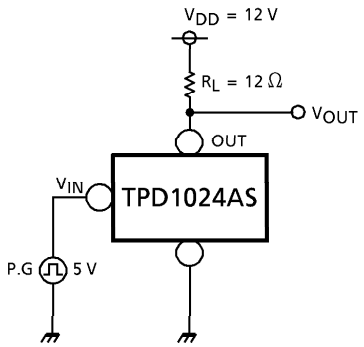
CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN	TYP.	MAX	UNIT
Input Voltage	V_{IN}	—	4.5	5	6	V

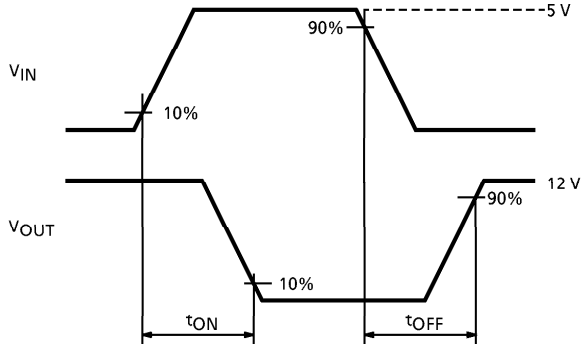
ELECTRICAL CHARACTERISTICS (T_j = 25°C)

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN	TYP.	MAX	UNIT
Drain-source Breakdown Voltage	$V_{(BR)\ DSS}$	—	V_{GS} = 0, I_D = 10 mA	40	—	—	V
Operating Supply Voltage	$V_{DD\ (OPR)}$	—	—	—	—	18	V
Current at Output Off	$I_{DSS\ (1)}$	—	V_{GS} = 0, V_{DS} = 40 V	—	—	3	mA
	$I_{DSS\ (2)}$	—	V_{GS} = 0, V_{DS} = 24 V	—	—	100	μA
Input Threshold Voltage	V_{th}	—	V_{DS} = 10 V, I_D = 1 mA	0.8	—	2.5	V
Input Current	I_{GSS}	—	V_{GS} = 5 V, at normal operation	—	—	300	μA
On Resistance	$R_{DS\ (ON)}$	—	V_{GS} = 5 V, I_D = 1 A	—	—	0.5	Ω
Overheating Protection	T_S	—	—	—	160	—	°C
Overcurrent Protection	I_S	—	V_{DS} = 12 V, V_{GS} = 5 V	—	3.5	—	A
Switching Time	t_{ON}	1	V_{DS} = 12 V, V_{GS} = 5 V, R_L = 12 Ω	—	50	—	μs
	t_{OFF}			—	10	—	μs
Diode Forward Voltage Between Drain and Source	V_{DSF}	—	I_F = 1.5 A	—	0.9	1.8	V
Avalanche Energy Rating	E_A	—	L = 10 mH, Single-shot pulse	30	—	—	mJ

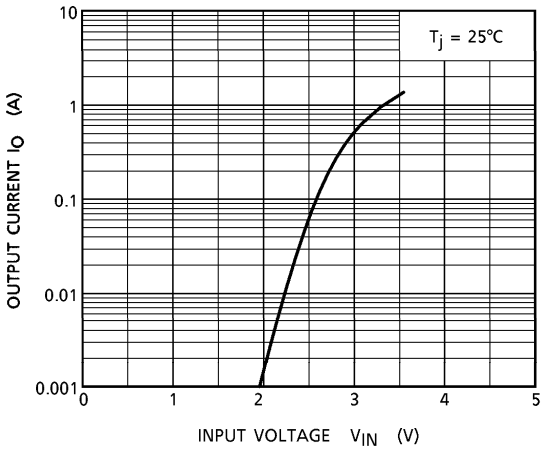
TEST CIRCUIT 1

Switching Time





I_O – V_{IN}



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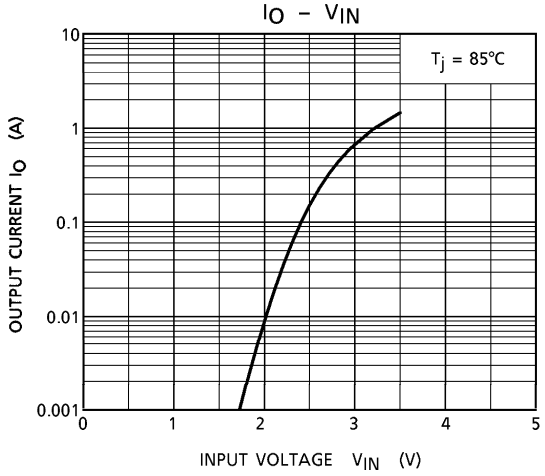
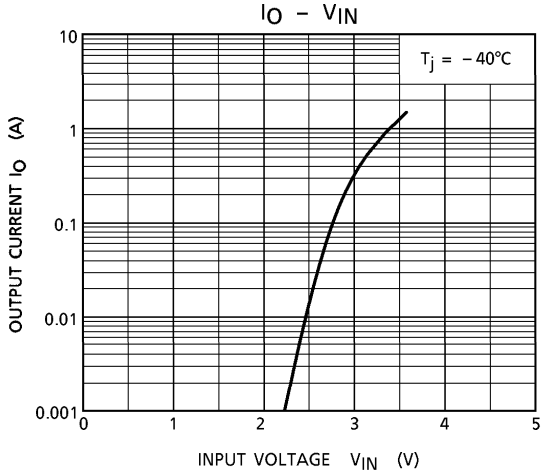
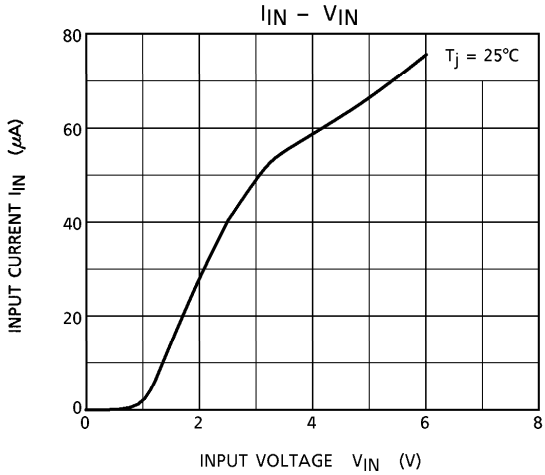


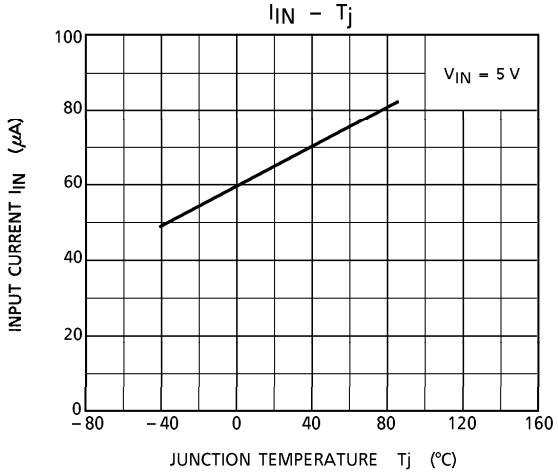
I_O – V_{IN}



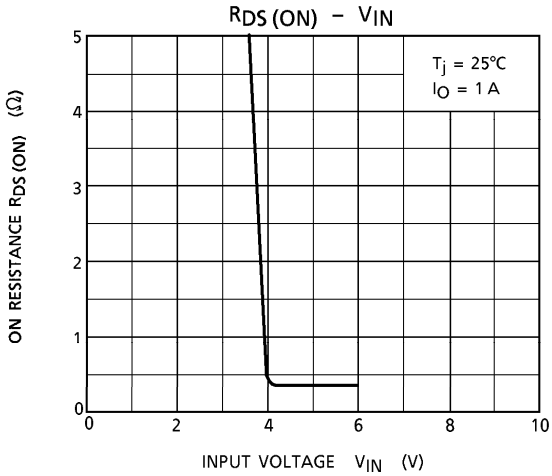
I_{IN} – V_{IN}



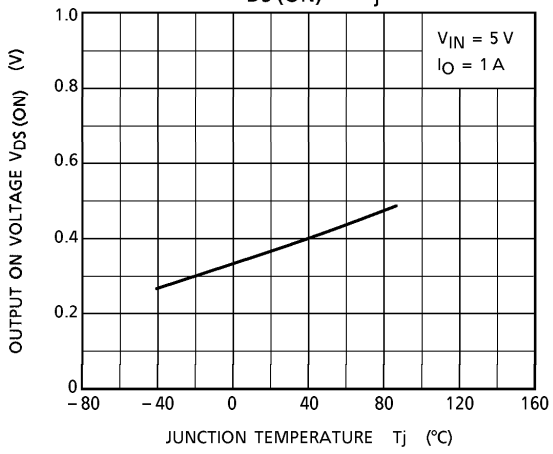
I_{IN} – T_j



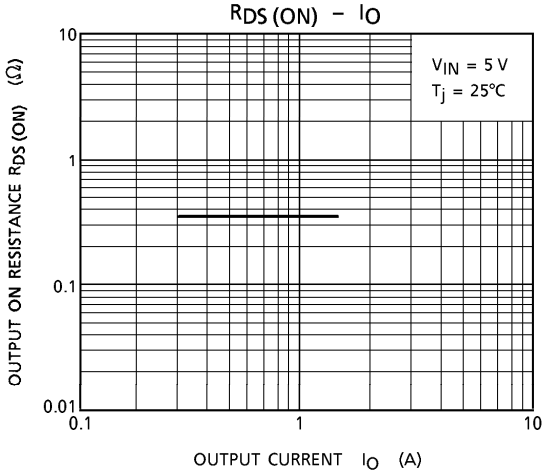
$R_{DS\,(ON)}$ – V_{IN}



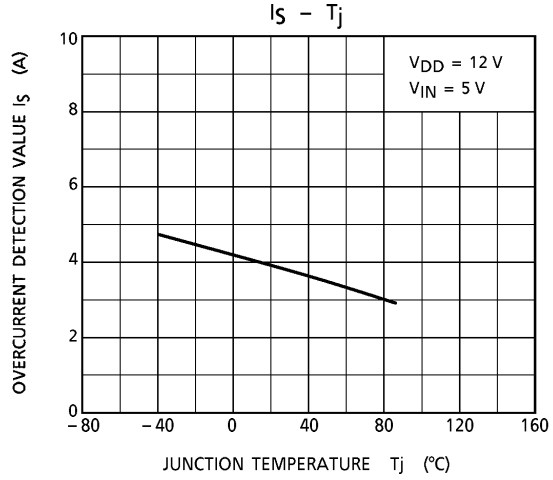
$V_{DS\,(ON)}$ – T_j



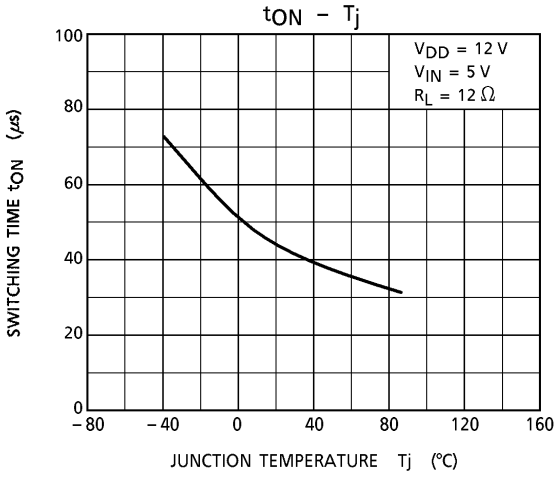
$R_{DS\,(ON)}$ – I_O



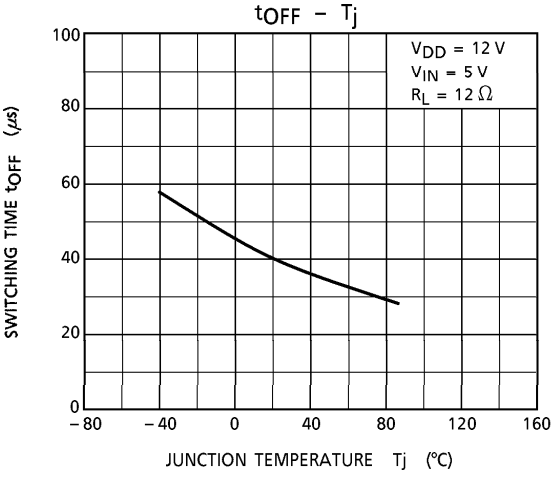
I_S – T_j



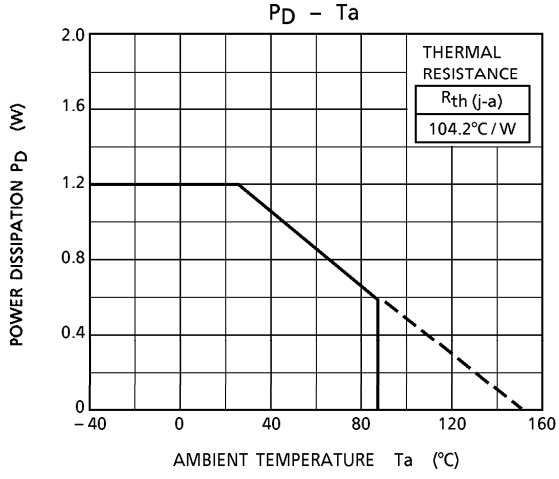
t_{ON} – T_j



t_{OFF} – T_j



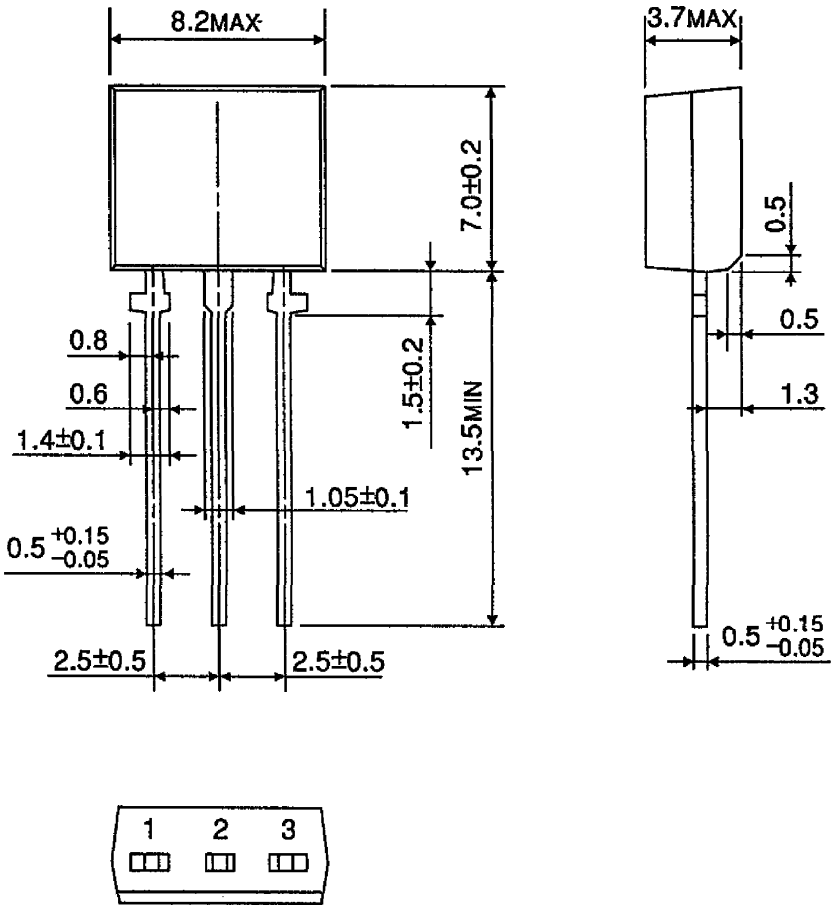
P_D – Ta



OUTLINE DRAWING

SIP3-P-2.50

Unit : mm



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